**BEE 271 Midterm, Spring 2017**

Name (please print): _____

This exam is closed book, closed notes, no cellphones, computers or calculators. It is unproctored. Please try sit next to students you don't normally. You have 2 hours to answer as many questions as you can. Some questions are easy and some are hard but each is worth the same 4 points, so pick and choose. Most correct answers can be short. If you need more space, additional sheets may be stapled to your exam. I will be outside the room if you need to discuss something.

Please copy the following statement *in your own handwriting* and s*ign your name* below it:

> On my honor, I will neither accept nor give unauthorized aid on this exam.

_____

_____

_____
Signed

1. Convert 193 base 10 to binary and hex following the procedure discussed in class. What is the minimum number of bits needed to represent this as an unsigned number?

2. Derive the simplest SOP equation that implements f( a, b, c ) = Σm( 3, 4, 5, 7 ) by using a Karnaugh map.

3. Derive the simplest SOP equation that implements f( a, b, c ) = Σm( 3, 4, 5, 7 ) by algebraic manipulation.

4. Derive the simplest POS equation for f(a, b, c) = ΠM(0, 1, 2, 6 ) using a Karnaugh map.

5. Derive the simplest POS equation that implements f( a, b, c ) = ΠM( 0, 1, 2, 6 ) by algebraic manipulation.

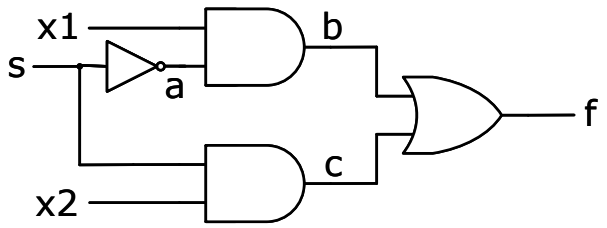
6. Draw diagrams of signed and unsigned n-bit numbers, numbering the bits. What do LSB and MSB stand for? Mark them and any sign bits on your diagrams. In an unsigned number, a 1 in position ***k*** would have what value?

7. What is the difference between overflow and carry?

8. Draw an example of bubble-pushing. What theorem is this based on?

9. What is the difference between an implicant, a prime implicant and an essential prime implicant?

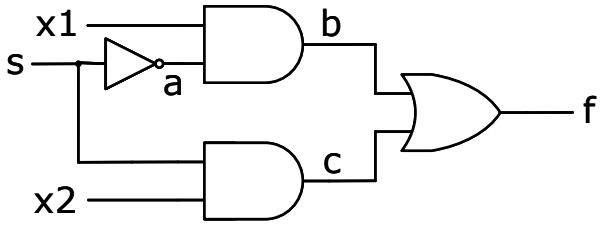
10. What does this circuit do? Is there a name for it? Write it as a Verilog module using only built-in gates and give it an appropriate name.

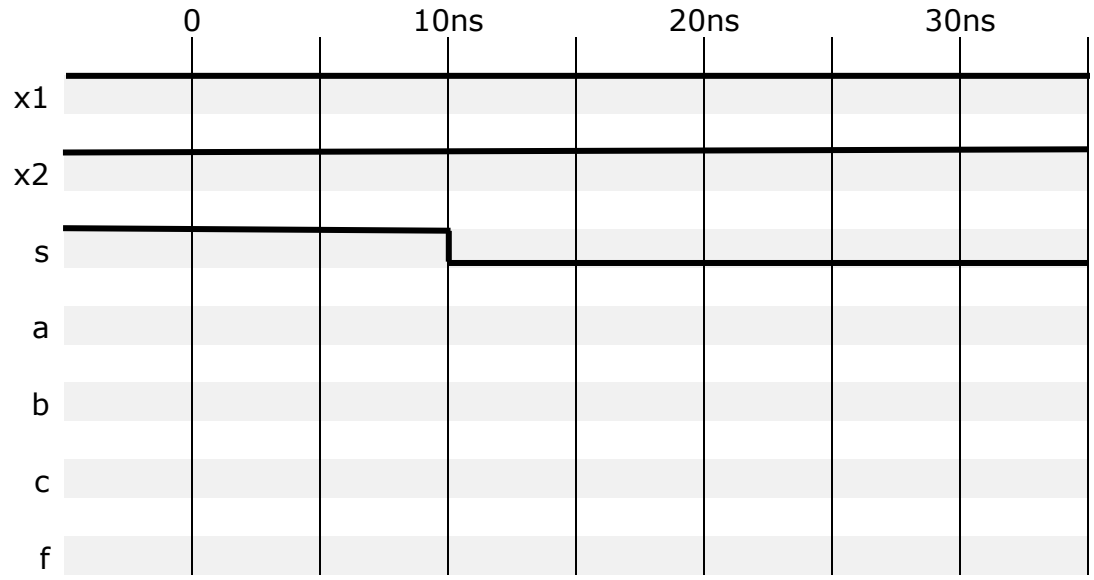



11. Write the same function as a Verilog module using continuous assignment.

12. Write the same function as a Verilog module using a behavioral specification.

13. Again referring to this circuit, fill in the timing diagram below, showing what happens to signals a, b, c and f. Assume all gate delays are 5 ns. You may not assume anything about the input signals prior to what's shown, so please indicate by crosshatching any signals that are unknown.



14. Draw simple sketches of Vin and Vout versus time for an inverter, showing how $t_{RISE}$, $t_{FALL}$, $t_{PLH}$ and $t_{PHL}$ are measured.

15. For the function g defined by this Karnaugh map, write the minterm equation, g = Σm(…) + D(…), identify the prime implicants and any essential prime implicants and then write the simplified SOP equation.

| g | | b1 b0 | | | |
|---|---|---|---|---|---|
| | | 00 | 01 | 11 | 10 |
| b3 b2 | 00 | | | d | |
| | 01 | | | 1 | d |
| | 11 | | | d | 1 |
| | 10 | 1 | 1 | d | |

16. For the function h defined by this Karnaugh map, write the Maxterm equation, h = ΠM(…) + D(…), identify the prime implicants and any essential prime implicants and then write the simplified POS equation.

| h | | b1 b0 | | | |
|---|---|---|---|---|---|
| | | 00 | 01 | 11 | 10 |
| b3 b2 | 00 | | 0 | | |
| | 01 | | d | | |
| | 11 | | d | 0 | |
| | 10 | | 0 | d | |

17. Implement f = a b c' + b' d' using a 16:1 multiplexer. If groups of inputs are all the same, you may simplify your drawing by indicating the list of inputs tied together.

18. Implement your 16:1 decoder solution to f = a b c’ + b’ d’ as directly as you can in Verilog using a case statement and the concatenation operator.

19. What is Shannon’s expansion? What is a co-factor?

20. Use Shannon’s expansion to implement f = a b c’ + b’ d’ using a 2:1 multiplexer, an AND gate and two inverters.

21. What are 3 different ways to represent a signed binary number? How would -17 (minus 17 decimal) be encoded as an 8-bit number under each method?

22. What are the steps to convert a 2's complement number to sign + magnitude so you make sense of it? Given the 2's complement value 16'hFF75, what is the signed decimal value?

23. Draw a circuit for a full-adder using two half-adders and any additional gates you need.

24. Write a Verilog module using a casex statement that takes a 4-bit value as input and outputs the number of ***trailing 1's***, e.g., 0111 → 3, 1011 → 2, 1100 → 0, etc.

25. Create a module in Verilog that adds a 5-bit ***signed*** binary number to a 9-bit ***unsigned*** binary number, producing a 10-bit ***signed*** result using the + operator and ***explicit sign extension*** using replication and concatenation (not the signed keyword). Can it ever overflow? Give an example to explain your answer.